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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,862	11/30/2000	Stephen E. Greco	00750414BA	3056

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EXAMINER

NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/725,862

Applicant(s)

GRECO ET AL.

Examiner

Joseph Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 January 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 27-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 27-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 November 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other:

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DETAILED ACTION

Claim Objections

Claims 32-35 are objected to because of the following informalities: "first protective layer" should be –"primary protective layer"—in order to be consistent with the claim language in the base claim 27. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 34 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation "the first protective layer on the sidewalls of the flowable oxide insulator is a low K dielectric" is not clearly and concisely disclosed in the specification in such a way that one having ordinary skill in the art could make and use. This limitation is not supported by the specification. ✓

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

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by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 27, 32, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Bai et al.

Regarding claim 27, Bai et al discloses an integrated circuit semiconductor device including "a substrate [40] having a substrate surface [readable on figure 4D], a flowable oxide insulator layer [41] upon said substrate surface; a trough [44], sidewalls [43,42] of said flowable oxide insulator layer [41], a primary protective layer [43] on said sidewalls of said flowable oxide insulator layer [41], said primary protection layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer [43] being impervious to copper extrusion, and a secondary protective layer [42] on said primary protection layer and on said substrate surface, said secondary protective layer [42] being electrically conductive [col. 8, line 40]". This is all illustrated in figure 4D.

Regarding claim 32, Bai et al discloses on figure 4D the first protective layer 43 is a barrier layer.

Regarding claim 34, Bai et al discloses on figure 4D the first protective layer on the sidewalls of the flowable oxide insulator is a low K dielectric.

Claims 27, 28, 32 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin et al.

Regarding claim 27, Lopatin et al discloses an integrated circuit semiconductor device including "a substrate [101] having a substrate surface [readable on figure 2], a flowable oxide insulator layer [116] upon said substrate surface; a trough [102],

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sidewalls [123,124] of said flowable oxide insulator layer [116], a primary protective layer [123] on said sidewalls of said flowable oxide insulator layer [116], said primary protection layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer [123] being impervious to copper extrusion, and a secondary protective layer [124] on said primary protection layer and on said substrate surface, said secondary protective layer [124] being electrically conductive [col. 1, lines 31-32]". This is all illustrated in figure 2.

Regarding claim 28, Lopatin et al further discloses "an oxidized FOX layer [117] upon said floatable oxide insulator layer [116], an oxide layer [108] upon said oxidized FOX layer, a conductor [102] in said trough, said conductor and said oxide layer forming an even planar surface, said conductor being in electrically communication with said secondary protective layer [124], and a nitride layer [126] upon said even planar surface". This is all illustrated in figure 2.

Regarding claim 32, Lopatin et al discloses on figure 2 the first protective layer 123 is a barrier layer.

Regarding claim 34, Lopatin et al discloses on figure 2 the first protective layer on the sidewalls of the flowable oxide insulator is a low K dielectric.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al as applied to claim 28 above, and further in view of Yew et al.

Regarding claims 29 and 30, Lopatin et al discloses substantially all the structure set forth in the claimed invention except the integrated circuit semiconductor device comprising a second damascene layer. Note that the second damascene layer is merely duplication of the first damascene layer of claim 27. However, Yew et al discloses on figure 2E the second damascene layer 226, 212 similar to the first damascene layer 222, 204. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lopatin et al by having the second damascene layer similar to the first damascene layer in the integrated circuit semiconductor device. The ordinary artisan would have been motivated to modify Lopatin et al in the manner described for the purpose of having a reduced parasite capacitance in the dielectric layers, thus assuring the performance of an IC device (col. 3, line 15-18).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al or Bai et al as applied to claim 27 above, and further in view of Kawanoue et al.

Regarding claim 31, Lopatin et al or Bai et al discloses substantially all the structure set forth in the claimed invention except the integrated circuit semiconductor device comprising a supplemental protective layer on primary protective layer, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor. However, Kawanoue et al discloses on figure 3C the integrated circuit semiconductor device having a supplemental protective

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layer 35 on primary protective layer 203, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lopatin et al or Bai et al by having a supplemental protective layer upon the protective layer, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor in the integrated circuit semiconductor device. The ordinary artisan would have been motivated to modify Lopatin et al or Bai et al in the manner described for the purpose of achieving a low via resistance, a low interconnect resistance and a high barrier effect in the integrated circuit semiconductor device (col. 10, line 30-36).

Claims 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al or Lopatin et al as applied to claim 27 above, and further in view of Ashley et al.

Regarding claims 33-35, Bai et al or Lopatin et al discloses substantially all the structure set forth in the claimed invention except the first protective layer having a thickness equal to or less than 20% of a thickness of the flowable oxide insulator. However, Ashley et al discloses on figure 6d the first protective layer 5 having a thickness less than 20% of a thickness of the flowable oxide insulator 3 (See the scale of figure 6b). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Bai et al or Lopatin et

al by having the first protective layer having a thickness equal to or less than 20% of a thickness of the flowable oxide insulator for the purpose of improving the electrical interconnect in the semiconductor device.

Response to Arguments

Applicant's arguments filed on 1/02/2002 have been fully considered but they are not persuasive.

With respect to claim 27, applicant argues that Bai et al does not disclose a low K or flowable oxide layer and the capturing layer of Bai et al is not "impervious to copper extrusion". However, Bai et al clearly discloses on *figure 4D* a flowable oxide layer and the capturing layer 43 is impervious to copper extrusion (col. 4, lines 1-3). Note that silicon dioxide is properly considered as flowable oxide layer in a broad term since there is no specific material relating to the so-called flowable oxide disclosed in the claimed invention. Furthermore, the capturing layer captures copper atoms that leak through the blocking layer and therefore the capturing layer is being impervious to copper extrusion.

With respect to claims 27-28, applicant argues that Lopatin et al does not disclose a secondary protective layer. However, Lopatin et al clearly discloses on figure 2 the secondary protective layer 124. This layer 124 is properly considered as secondary protective layer in the sense that there is no specific material relating to the so-called secondary protective layer disclosed in the claimed invention.

With respect to claims 29-31, applicant argues that there is no *prima facie* demonstration of obviousness of the subject matter of the claimed invention. However, In response to applicant's argument that the examiner's conclusion of obviousness is

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based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
February 26, 2002



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800